IN THE SPECIFICATION

1. Please amend the paragraph starting on page 1, line 6 of the application as follows:

The present invention relates generally to trimming of analogue filters in integrated circuits. More particularly, the invention relates to a method for automatically altering a magnitude of at least one component value in an analogue filter ~~according to the preamble of claim 1~~ and an automatic adjusting circuit for calibrating an analogue filter in an integrated circuit ~~according to claim 15~~. The invention also relates to a computer program ~~according to claim 13 and a computer readable medium according to claim 14~~.

2. Please amend the Abstract on page 16 of the application as follows:

An adjustable phase shifter generates a phase shifted reference signal by introducing a phase shift in a reference signal. A phase detector identifies a phase difference between the reference signal and the phase shifted reference signal. A control signal generator generates a plurality of control signals, each of which causes the adjustable phase shifter to adjust a magnitude of at least one component value in the adjustable phase shifter. The phase shift introduced by the adjustable phase shifter is based at least partially on the magnitude of the at least one component value in the adjustable phase shifter. The control signal generator also selects one of the control signals, where the selected control signal causes the adjustable phase shifter to produce the phase shifted reference signal such that the phase difference attains a specified value. The analog filter adjusts a magnitude of at least one component value in the analog filter based at least partially on the selected control signal.

~~The invention relates to trimming of analogue filters (201) in integrated circuits by means of an automatic adjusting circuit. A local oscillator (202) in the automatic adjusting circuit provides a periodic reference signal (R) to an adjustable phase shifter (203), which on basis thereof, produces a periodic phase shifted signal (R*). A phase detector (204) receives both the periodic reference signal (R) and the phase shifted period signal (R*) and produces a test signal (T) in response to a phase difference between the periodic reference signal (R) and the periodic phase shifted signal (R8). A lowpass filter (205) receives the test signal (T) and generates a level signal (T.sub.DC) relative a~~

~~reference level, e.g. representing a zero voltage. A digital signal processor (207) produces a primary control signal (C.sub.S), having a serial format, on basis of the observation signal (M). A serial-to-parallel converter (208) converts the primary control signal (C.sub.S) into a control signal (C.sub.P) having a parallel signal format. The control signal (C.sub.P) influences a magnitude of at least one component value in the adjustable phase-shift between the periodic reference signal (R) and the periodic phase shifted signal (R*) attains a calibrated value being as close as possible to a desired value. A latch (210) forwards at least one signal element of the control signal (C.sub.P) for setting of at least one component value in the analogue filter (201) in accordance with a setting of at least one component value in the adjustable phase shifter (203) which produces the calibrated value.~~